Prior Art Rejections

1. *Itoh*

Claims 1 and 3-4 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Itoh et al.* (U.S. Patent 5,585,817). This rejection is respectfully traversed.

By way of review, independent claim 1 is directed to an image display apparatus comprising: an imaging section having photoelectric conversion devices arranged in the form of a matrix; and a display section having display devices arranged in the form of a matrix. The imaging section of claim 1 sequentially outputs signals generated by the photoelectric conversion devices in parallel column by column of the matrix. The display section of claim 1 displays an image represented by signals applied thereto at the time of applying driving pulses, applies the signals output in parallel from the imaging section to display devices column by column, and supplies the driving pulses line by line in a predetermined order. As shown in Fig. 1, illustrating an embodiment on which claim 1 reads, the imaging section outputs the signals from the plurality of columns of the imaging section matrix without conversion to serial form, thereby reducing the transmission rate of the signals.

Independent claim 4 is directed to an image display apparatus comprising: an imaging section having photoelectric conversion devices arranged in the form of a matrix; a signal conversion section; and a display section having display devices arranged in the form of a matrix. The imaging section of claim 4 sequentially outputs signals generated by the photoelectric conversion devices in parallel column by column of the matrix. The signal conversion section of claim 4 processes the signals output from the imaging section in parallel column by column and outputs the processed signals in parallel. The display section of claim 4 applies the signals output in parallel from the signal conversion section to the display

devices column by column and supplies driving pulses for image display line by line in a predetermined order.

In maintaining the rejection of independent claims 1 and 4 based solely on *Itoh*, the Examiner replies to the arguments set forth in the Amendment dated January 28, 2002 by stating that:

> Applicant argues that Itoh et al. (USPN 5585817) does not disclose generating a parallel column by column output from the image section. Applicant also argues that Itoh does not disclose a display section which applies output signals in parallel. However, as will be shown in the rejection below, Itoh teaches the division of a photo detective portion (109) into multiple blocks. Itoh teaches outputs V(out 1), V(out 2) for blocks 109' and 109" respectively. Itoh further teaches parallel scanning block by block as well as an image input which can be performed by a single scanning circuit. In addition Itoh teaches that an image input section and an image display section are constructed into a unit. Itoh illustrates in detail the scanning method during image inputting process as shown in Fig. 4. See Fig. 5, col. 6, lines 9-25 and col. 3, lines 15-19, 57-59.

Applicant notes, however, that the image input section 20 of *Itoh* is adapted to develop the signals produced by the photodetective portion 109 in line sequential and in column sequential fashion, as seen clearly from the waveform for V_{out} seen in Fig. 4. Although the photodetective portion 109 includes blocks 109' and 109", as seen in Fig. 5, for producing outputs V_{out1} and V_{out2}, respectively, each of these blocks 109' and 109" is adapted to output the signals generated by the associated subportion of the photodetective portion 109 in line sequential and in column sequential fashion for that block. In other words, the image input section 20 of *Itoh* is not adapted to output the signals generated by the photodetective portion 109 in parallel from the imaging section to display devices column by column. Regarding the Examiner's statement that "Itoh further teaches parallel scanning block by block as well as an image input which can be performed by a single

scanning circuit," the device of *Itoh*, when displaying an image, selects the pixels arranged in the form of a matrix one by one in line sequential and column sequential fashion so that data is sequentially written into the selected pixels, as seen at col. 5, lines 8-11. Thus, the pixels, or liquid crystal portions, are apparently driven one by one in sequence to display an image. In contrast, the display section defined in claims 1 and 4 applies signals to the display devices arranged in the form of a matrix column by column in parallel (such that the display units included in a display line are driven simultaneously).

Furthermore, with regard to the Examiner's statement that "Itoh teaches that an image input section and an image display section are constructed into a unit," *Itoh* teaches that the apparatus for inputting/outputting an image is adapted, when an image is to be input, to sequentially feed the thin film transistors 101 arrayed in the form of a matrix with the high level voltage and the high level voltage pulses to turn the pixels on sequentially. See e.g., col. 5, lines 12-27. Therefore, it is not possible to display an image when an image is being input. By contrast, with the image display apparatus defined in claims 1 and 4, an image captured by the imaging section can be immediately displayed by the display section.

At least for these reasons, Applicant respectfully submits that the asserted grounds of rejection fails to establish *prima facie* obviousness of independent claim 1 or independent claim 4. Furthermore, claim 3 patentably distinguishes over *Itoh* at least for depending from claim 1.

In view of the above, Applicant respectfully requests reconsideration and withdrawal of the Examiner's rejection under 35 U.S.C. § 103 based on *Itoh*.

2. *Itoh - Sasaki*

Claims 2 and 5-11 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Itoh* in view of *Sasaki* (U.S. Patent 5,140,440). This rejection is respectfully traversed.

By way of review, independent claim 8 is directed to an image display apparatus comprising: an imaging section having photoelectric conversion devices arranged in the form of a matrix; a signal conversion section for processing signals output from the imaging section; and a parallel-to-serial conversion section. The imaging section of claim 8 sequentially outputs signals generated by the photoelectric conversion devices in parallel column by column of the matrix. The signal conversion section of claim 8 processes signals output in parallel from the imaging section column by column and outputs the process signals in parallel. The parallel-to-serial conversion section of claim 8 converts the signals output in parallel from the signal conversion section to serial signals.

In rejecting independent claim 8, the Examiner relies on *Sasaki* as allegedly teaching the parallel-to-serial conversion section recited in the claim. As discussed above, however, *Itoh* fails to disclose or suggest an imaging section as recited in independent claim 8. The Examiner's reliance on *Sasaki* fails to make up for this deficiency of *Itoh*. Therefore, *Sasaki*, taken alone or in combination with *Itoh* (assuming these references are combinable, which Applicant does not admit), fails to establish *prima facie* obviousness of independent claim 8.

Independent claim 10 is directed to a display apparatus comprising: a serial-to-parallel conversion section for converting signals serially input thereto to parallel signals; a signal conversion section for processing the signals output in parallel from the serial-to-parallel conversion section column by column; and a display section having display devices arranged in the form of a matrix. The display section of claim 10 displays an image represented by

signals applied thereto at the time of applying driving pulses and applies the signals output in parallel from the signal conversion section column by column.

In rejecting independent claim 10, the Examiner relies on *Sasaki* as allegedly teaching the serial-to-parallel conversion section recited in the claim. Applicant submits, however, that neither *Itoh* nor *Sasaki* teach or suggest a signal conversion section as recited in independent claim 10, which processes the signals output in parallel from a serial-to-parallel conversion section column by column and outputs the processed signals in parallel. Consequently, Applicant submits that *Sasaki*, taken alone or in combination with *Itoh* (assuming these references are combinable, which Applicant does not admit), fails to establish *prima facie* obviousness of independent claim 10.

Dependent claims 9 and 11 define over the asserted combination of *Itoh* and *Sasaki* at least for depending from claims 8 and 10, respectively, as well as on their own merits.

Additionally, Applicant notes that the apparatus of *Itoh* integrates an image display section and an image input section into a single unit to accomplish a small-size device for inputting/outputting an image. On the other hand, Applicant's claimed invention obviates a parallel-to-serial conversion, which would otherwise be required in an imaging section, by outputting signals from the imaging section in parallel column by column and inputting the signals to the display section in parallel column by column. Further, in accordance with Applicant's invention, the signals developed from the imaging section are processed in parallel, thus enabling the data processor to operate at a lower frequency to reduce electric power consumption. Neither *Itoh* nor *Sasaki* teaches or suggests an apparatus that achieves these results.

At least in view of the above, Applicant respectfully requests reconsideration and withdrawal of the Examiner's rejection under 35 U.S.C. § 103 based on the asserted combination of *Itoh* and *Sasaki*.

CONCLUSION

Should there be any outstanding matters which need to be resolved in the present application, we respectfully request the Examiner to contact the undersigned at (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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